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A Novel Bidirectional T-type Multilevel Inverter for Electric Vehicle Applications

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***Abstract*—This paper introduces a new configuration of bi-directional multilevel converter in electric vehicle (EV) applications. It has multilevel DC-DC converter with a direct current (DC) link capacitor voltage balance feature. The multilevel DC-DC converter operates in bi-directional manner, which is a fundamental requirement in EVs. Compared to the conventional configurations, the proposed one only implements two extra power switches and a capacitor to balance the voltage of the T-type MLI capacitor over a complete drive cycle or at fault conditions. Therefore, no extra isolated sensor, control loops and/or special switching pattern are required. Moreover, the proposed configuration due to the high frequency cycle-by-cycle voltage balance between C_n and C_p the bulky electrolytic capacitors used in T-type MLI are replaced with longer life more reliable film capacitors. This will result in a size and weight reduction of the converter by 20%. This allows more real estate for the EV battery in the chassis' space envelope; to increase its capacity. The proposed configuration is tested and validated using a Matlab/Simulink simulation model. A laboratory prototype 1 kW is built to provide the proof of concept results as well.**

Keywords—Multilevel inverter, T-type MLI, Multilevel DC-DC converter, bi-directional converter, Capacitor voltage balance, natural voltage balance;

I. INTRODUCTION

Many multilevel inverter topologies has been introduced to address different types of applications [1] [2] [3]. Generally, multilevel inverters either rely on isolated dc power sources or split capacitors connected to a single dc power source to synthesis its stepped output voltage levels. The first type is more reliable but require as mentioned increasing number of dc power sources and power switches such as cascaded H-bridge multilevel inverter. On the other hand, the split capacitor based MLI such as neutral point clamped NPC MLI [4], flying capacitor FC MLI [5] and T-type MLI [6] [7] required lower number of power components. Nonetheless, as the voltage across each capacitor is relaying on an ideal natural balance, their voltages in practical are susceptible for voltage drifting which leads to voltage imbalance operations.

In electric vehicle applications, the three-phase inverter in propulsion system is fed by a bi-directional DC-DC converter [8] [9] [10]. It controls the dc bus voltage by regulating its voltage to be at the level required to allow the power to flow to the electric machine in motoring mode over the designed range of modulation index (mi). In breaking mode (regenerative), the bi-directional converter stepped the DC voltage to allow the power to flow in reverse direction from the electric machine back to the utility grid or electrical storage units as in electric vehicle. Based on the power source connected to the propulsion system, the bi-directional converter can be designed as boost converter in motoring mode and buck converter in during breaking, or vice versa.

Although conventional dc-dc converters are very reliable in controlling the dc bus voltage, it is not always the case when are connected to a multilevel inverter [11], [12]. As mentioned, multilevel inverter that is connected to a single dc power source is relying on split capacitor as an input stage to produce its sub-level output voltages. Such arrangement is susceptible to unbalanced capacitor voltages and hence voltage deviation of the neutral point [1]. Therefore, an extra circuitry with or without control loop is to be added to ensure a balanced voltage on the capacitors and balance the neutral point [13], [14] . Another solution is applying a modified switching scheme [15] that chooses between a different set of switching state to reestablish the voltage balance once detected.

Nonetheless, modified switching as presented in [16] [17] [18] can successfully mitigate this issue. Without a feedback controller, the converter still susceptible to temporary faults that affected the balance in capacitor voltages. A voltage balance circuit offers a much robust and accurate method to balance the voltage on the capacitors and control inverter's neutral point. While the first method is preferable when it comes to the power train cost and space envelope. The second one can recover the balance and control neural point against wider range of faults. With proper design, it also has advantage of reducing the control complexity and eliminate the need for isolate voltage sensors, which not only affect the cost but the inverter lifetime as well.

Many techniques are presented to control the capacitor voltages and the neutral point in split capacitor based multilevel inverters. In [16], a hybrid space vector modulation SVM is introduced. It integrates two modulation techniques to cover the total range of modulation index. An optimized SVM at low modulation which results in low total harmonics distortion and reduce the switching states. The high modulation area is covered by simplified SVM which reduce the complexity of the required calculations. Such technique sustain the balance in the capacitor

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voltages and allow for operating in both motoring and breaking modes. On the other hand, it requires an addition of isolated sensors and a controller that can handle the necessary calculations. Hence, increase the system cost and reduce its reliability. Similar balancing techniques based on the modified modulation are also introduced in [17] and [18], which also suffers from the same drawback by adding more isolated voltage sensors and control loops.

In conclusion, the modified modulation based techniques do not require adding an extra components in terms of power components (active/passive switches, capacitor and/or inductors). Thus, it has been seen as an optimum solution. However, it requires adding extra sensors and control loops if a wide range of operation and fault tolerance are to be achieved. Moreover, their ability to control and equalize the capacitors' voltages are limited by the redundancy states that are offered by the construction of multilevel converter itself.

As mentioned, capacitors' voltage balance in multilevel inverter can also be achieved by adding an extra circuitry between the input power source (batteries connected to a bi-directional in EV) and the MLI, as shown in Fig.1. The added circuitry can be an active circuit as introduced in [19]. In [19], the introduced voltage balancing circuit consists of two active power switches, three diodes and coupled inductors per two capacitors. Although the overall configuration is able to reduce the magnetic flux fluctuation in the coupled inductor as well as uniformly distribute the power losses across the power switches. It requires an addition of feedback control loops, harmonic injection and as mentioned increasing number of components and can only operate in applications without regenerative breaking. Therefore, it is suitable in medium voltage drive application, but less desirable in low voltage application as in electric vehicles.

Similarly, in [20] a capacitor based auxiliary circuit is introduced to balance capacitor voltage in 5-level NPC multilevel inverter. Its generalized form consists of twenty-one active switches and six auxiliary capacitors but a simplified version is also introduced based on one auxiliary capacitor and twelve active switches. However, it suffers from the same issues as it requires adding more components and control which increase the system complexity. Moreover, it does not limit the operation to motoring only as in [19]. In [21] a novel multilevel converter based on the same principle is introduced, which although, solves the capacitors voltages imbalance in MMC, its contracture does not allow for four quadrant machine drive.

In [22] the capacitors' voltages are balanced using three active switches and two inductors to achieve voltage equalization across three input capacitors. These components configure two-buck converters, which can successfully control the capacitors' voltages. For such configuration, this balancing circuit requires a adding more feedbacks and control loops. Moreover, compared to the capacitors based voltage balancing circuit, the inductors based on are less preferable.

The multilevel dc-dc boost converter originally introduced in [23] [24] [25] can only operate as uni-directional boost converter which make it impractical in electric machine drive applications especially in EV. Therefore, the proposed converter configuration modified its structure by replacing the clamping diodes connected with C_M by two active power switches. These two switches are operated in a complementary manner and in conjunction with the boost converter synchronous switches as shown in Fig. 2. So, the simplicity of the original contracture is reserved as well as the number of controlling signal. Therefore, the proposed converter configuration is able to achieve a bi-directional operation where the input voltage is boosted in motoring mode, and the combined capacitors' voltage is bucked in breaking (regenerative) mode.

This paper is organized as follow, first the operation of the proposed configuration has been explained in details, including the switching states in different operating modes. Then, the converter's capacitor sizing is discussed. Finally, the validity of the proposed configuration has been investigated using both simulation model and experimental prototype.

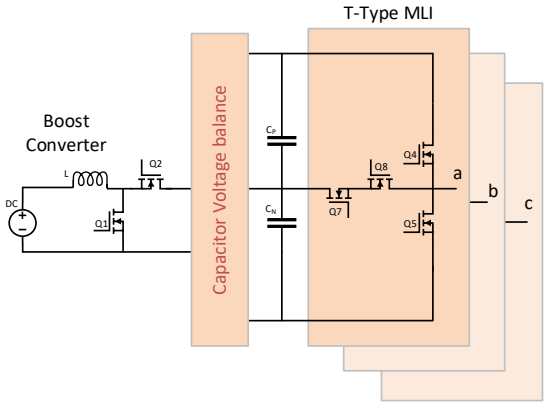

Fig. 1. The conventional configuration, a dc-dc converter connected to a voltage balancing circuit before connected to the T-type MLI.

II. PROPOSED SYSTEM CONFIGURATION

Conventionally, from the propulsion system design point of view, the dc input power source is connected to the bi-directional dc-dc converter, which controls the voltage of the dc bus. The voltage balancing circuit is placed between the output of the dc-dc converter and the input of the multilevel inverter.

On the other hand, in the proposed configuration, the input dc power source (such as batteries in EV) is connected to a bi-directional multilevel dc-dc converter as shown in Fig. 2. Its split output capacitors supplies the multilevel inverter is with the sub-level voltages requires to generate its ac output voltage. The added capacitor C_M in the multilevel bi-directional dc-dc converter acts an intermediate energy storage. It transfers the excess electrical energy from the higher capacitor C_P to the lower one C_N and vice versa. Hence, the converter can achieve natural voltage balance between C_P and C_N without any feedback or added control loop.

Although multilevel dc-dc converter utilizes two extra switches and a capacitor which affects power train cost and size. It introduces an advantage of increasing its voltage

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boosting gain by two for the same duty cycle in conventional boost converter. It is done without increasing the reverse blocking voltage seen by any of the power switches. In other words, for the same output voltage, multilevel dc-dc converter utilized power switches with half of the blocking voltage V_b, and operates in half of the duty cycle D in comparison with the conventional boost converter.

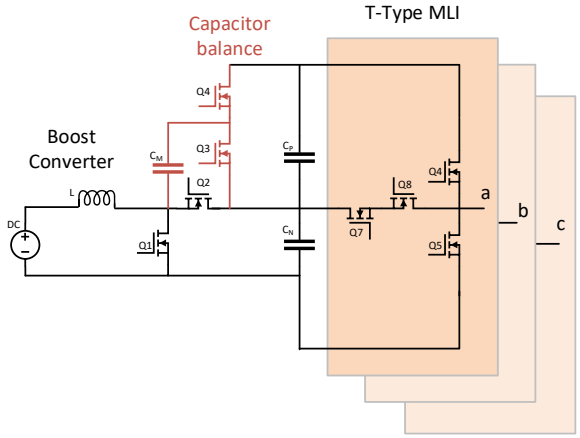


Fig. 2. The proposed configuration, a multilevel bidirectional DC-DC converter connected to the T-type MLI.

A. *Circuit operation*

The operation of the proposed converter configuration is divided based on the two modes of operation into 1) Step-up mode in in machine motoring state; and 2) bucking mode in machine breaking (regenerative) state. It is important to notice that the boost converter is operating in continuous conduction mode where the average inductor current is more than its ripple. Fig. 3 (a) and (b) show the electrical power flow from the input dc voltage to the lower capacitor C_N to the C_M and to the upper capacitor C_P over a complete switching period T_S. In such case, the multilevel inverter operates in typical condition where the power delivered by each capacitor C_N and C_P are qual. Hence, the boost converter always pushes the power to C_N which is transferred to C_P via C_M as will be explained.

Fig. 3 (a) shows the first state where $DT_S > t > 0$. The switch Q1 is ON while Q2 is OFF allowing the inductor current to increase i_L. At the same time, Q3 is ON and Q4 is OFF, connecting the middle capacitor C_M to C_N. Because of being connected directly to the boost converter, C_N has a higher voltage V_{CN} than C_M voltage V_{CM}, thus, the power is transferred from C_N to C_M as shown by the arrows. The second state is shown in Fig. 3 (b) where $T_S > t > DT_S$, in which, Q1 is OFF while Q2 is ON. The inductor starts to discharge through Q2 to C_N which increases its voltage V_{CN}. At the same time, the power is transferred form C_M (which is being charged at a higher voltage ($V_{CM} = V_{CN}$) from C_N) to C_p by connecting Q4 and disconnecting Q3.

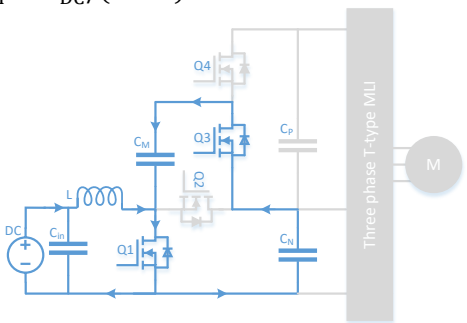
The power flow between C_N, C_M and C_P can be reversed as shown in Fig. 3 (c) and (d). For example the voltage across C_N is lower than C_p ($V_{CN} < V_{CP}$). This can occurs due to a temporary switching fault. In such case, at $DT_S > t > 0$ the power will be transferred from C_M to C_N as shown be the arrows in Fig. 3 (c). Consequently, when C_M is connected to C_P it will be charged though Q4 as shown in Fig. 3 (d) and the cycle will be repeated. In regenerative mode, the electric machine acts as a generator forcing the power back to the dc bus. Therefore, in order to increase the efficiency of the driving system, the bi-directional operates as a buck converter to recovers this energy back to the DC power source. Fig. 3. (a) and (b) show the operating states over a complete switching period T_S.

In motoring mode, the first state occurs at $DT_S > t > 0$ in which Q2 and Q4 are ON while Q1 and Q3 are OFF. The regenerative power is transferred from C_N to the DC source and charging the inductor L and the capacitor C_{in}. Meantime, C_p is charging to C_M through Q4 as V_{CP} is now higher that V_{CM}, as shown in Fig. 3 (a).

The second state occurs at $T_S > t > DT_S$, where, Q1 and Q3 are ON while Q2 and Q4 are OFF. While Q1 allows the power to transfer from the inductor L and the input capacitor C_{in}, Q3 connects C_M to C_N as shown by the arrows in Fig. 3 (b). Due to the power transfer from C_N to the input DC its voltages V_{CN} is reduced compared to V_{CP} and V_{CM}. Thus, C_M charges C_N which increases its voltage again.

Nonetheless, it is possible for the power flow between C_N, C_M and C_P to be reversed as shown in Fig. 4 (c) and (d). For example when the voltage across C_N is higher than C_p ($V_{CN} > V_{CP}$). In such case, at $T_S > t > DT_S$ the power will be transferred from C_N to C_M as shown be the arrows in Fig. 4 (d). Consequently, when C_M is connected to C_P it will charge it though Q4 as shown in Fig. 4 (c) and the cycle will be repeated.

It can be notice that, the converter can now work as bi-directional converter instead of being only able to work as a uni-directional one. In typical operations, the dc-dc converter (in boosting mode) charges the lower capacitor C_N at output voltage $V_{CN} = V_{DC}/(1-D)$. C_M acts as an intermediate storage that charges from C_N and charge C_P at the same voltage, all within once switching cycle. At the bucking mode, C_M is charged from C_P then charges C_N which ensures the voltage balance in reverse power flow. Therefore, the balance between the capacitor is sustain and the voltage across the dc bus equals $V_{CP} + V_{CN} = 2V_{DC}/(1-D)$ (in boosting mode). It is worth to mention that the reverse voltage seen by any of the power switched Q1, Q2, Q3 and Q4 is clamped to the $V_{rev} = V_{CN} = V_{CP} = V_{DC}/(1-D)$.



(a)

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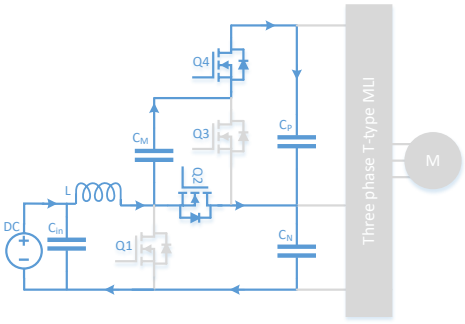

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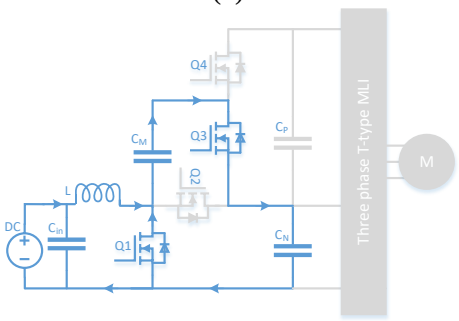

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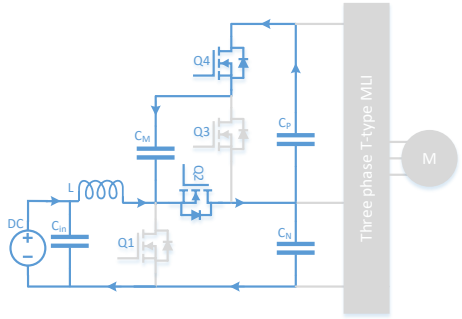

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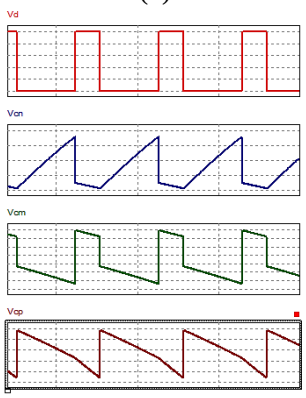
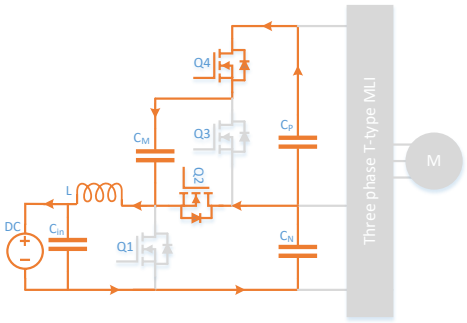


(e) Capacitors' voltages waveforms and Q1 gating signal in steady state.

Fig. 3. The operation of the proposed configuration in boosting mode in motoring drive mode.

While the output voltage at the dc bus = $2V_{DC}/(1-D)$. Fig. 3 (e) shows the capacitors' voltages theoretical waveforms with respect to Q1 gating signal in steady state which further demonstrate the capacitor charging / discharging to achieve voltage balance.



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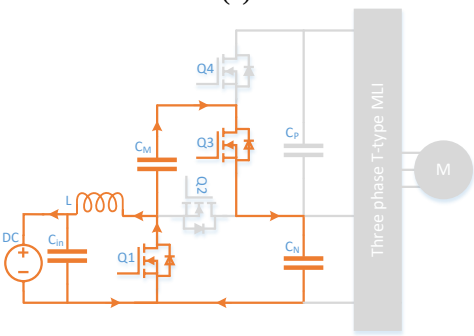

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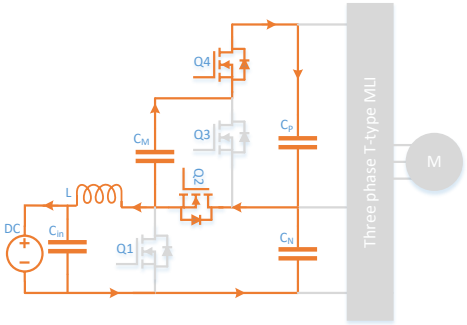

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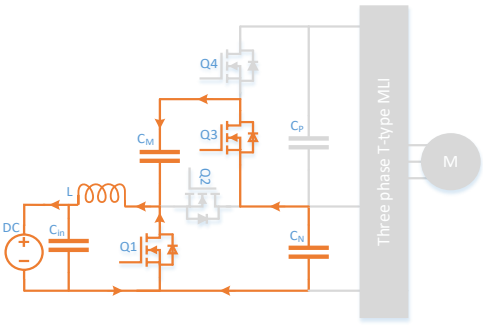

(d)

Fig. 4. The operation of the proposed configuration in bucking mode in breaking (regenerative) drive mode.

Finally, it is important to note that as two capacitors charged at different voltage levels are come to contact, an inrush current spike is generated. Therefore, a small inductance is added in series with the middle capacitor C_M to limit such current. Here

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a 1uH inductor is enough to limit the inrush current to about the load nominal current at switching frequency $f_s = 50kHz$.

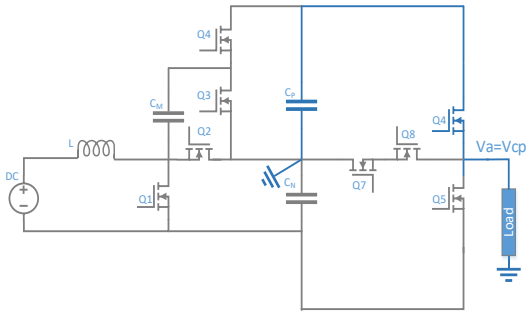
B. Capacitor design

Fig. 5 (a) to (c) shows the output ac voltage generation at the load terminals for one phase (phase a) of T-type multilevel inverter. In the positive half cycle, the load is connected to capacitor C_P through Q4, as shown in Fig. 5 (a). While in the negative half cycle the load is connected to C_N through Q5, as shown in Fig. 5 (b). The zero voltage level is generated by clamping the load using the bi-directional switch configured by Q7 and Q8, as shown in Fig. 5 (c).

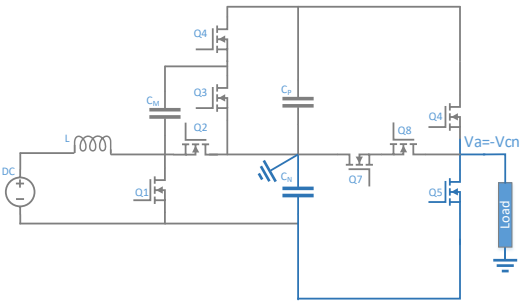
Therefore, the capacitance of C_P and C_N should be high enough to supply the load rated power and maintain their voltage ripple at minimum. The capacitance can be calculated as follow:

$$C = \frac{P}{2*\pi*f*dv*V^2} \quad (1)$$

Where, P is the load power, V is the load voltage, dv is the voltage ripple and finally f is the frequency of the load power variation.



(a)



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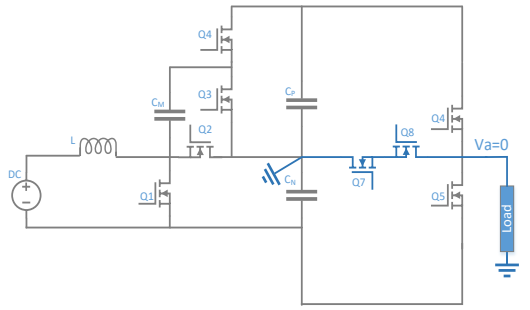


(c)

Fig. 5. The switching states of the T-type multilevel converter.

Unlike three phase voltage source inverter, in typical three-phase T-type multilevel inverter, the capacitors are designed to compensate for the variation in the load power at low frequency $f = 180Hz$ (for 60Hz system) with voltage ripple =10%, as shown in Fig. 6. Nonetheless, because of the voltage ripples seen across the capacitors (V_{CP} and V_{CN}) are 180° out of phase, the resultant will be a dc voltage level $V_{DC_{bus}}$ with only the high frequency ripple of the bi-directional converter [26] as shown in Fig. 7 (a).

Therefore, even tough the bi-directional converter operates at higher switching frequency compared to the multilevel inverter. It can not detect and compensate for the capacitors voltage variation due to the low frequency power variation.

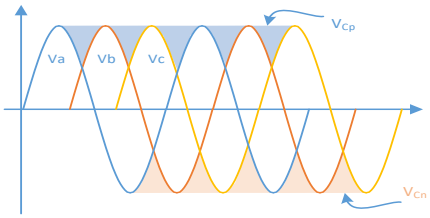
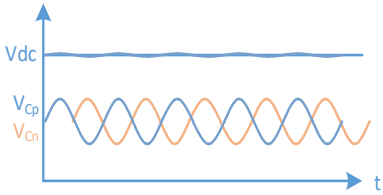
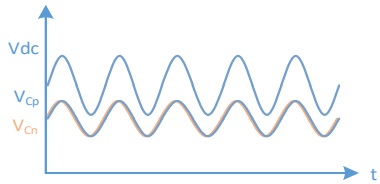


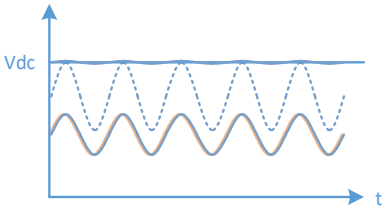
Fig.6. Compensate for the variation in the load power at low frequency $f = 180Hz$ (for 60Hz system) in T-type MLI.



(a) Capacitor voltages of T-type MLI connected to a conventional bi-direction DC-DC converter



(b) The capacitor voltages of T-type MLI in the proposed configuration.



(c) The capacitor voltages of T-type MLI in the proposed configuration after compensated by the controller.

Fig. 7. The variation of the dc bus $V_{DC_{bus}}$ voltage and capacitors' voltages.

Thus, as mention, it limits the ability to reduce the capacitance values of C_P and C_N in order to replace the conventional electrolytic capacitors with film capacitors. For example, if the dc bus capacitors are designed based on

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equation (1), then, for a 120kW, 750V dc bus voltage with dv=10% and rated speed at 60Hz. The minimum values of the dc bus capacitors is 1.9mF which is only available in range of the electrolytic capacitors.

In the proposed configuration, on the other hand, the voltage of both capacitors (C_p and C_N) V_{CP} and V_{CN} are balanced by the middle capacitor C_M as shown in Fig. 4. That means in every switching period T_s of the bi-directional converter, the voltage across all the capacitors are equalized, $V_{CN} = V_{CM} = V_{CP}$. Hence, all the capacitors voltage ripples are in phase and the resultant voltage ripple at $V_{DC_{bus}}$ is increased, as shown in Fig. 7 (b). Although, this is consider a disadvantage, it allows the feedback controller of the bi-directional converter to detect and compensate for the voltage variation. Thus, it maintains all voltages of all capacitors at their reference values as shown in Fig. 7 (c).

Therefore, the capacitance of each capacitor is chosen based on the design of the high frequency bi-directional converter to filler its switched voltage, which can lead to implement capacitors with significantly lower capacitance. Thus, electrolytic capacitors normally associate with such multilevel inverter can be replaced with film capacitors that offers much higher life-time and stable performance [27], [28]. This is all done without affecting the dc bus voltages or introduces unwanted harmonics to the drive train. Equation (2) is then used to calculate the minimum capacitance required by any high frequency boost converter as follow:

$$C = \frac{V\,D}{2\,f_s\,dv\,R} \qquad (2)$$

Where V is the $V_{DC_{bus}}$, D is the boost nominal duty cycle, f_s is its switching frequency, dv is the allowed voltage ripple in voltage (V) and R is the load equivalent Ohmic resistance. Thus, following the same input of the pervious example, (with 200V input voltage), the required capacitance is 15 uF which is within range of film capacitors available in the market. Nonetheless, as the low frequency ripple is to be compensated from the boost input side, such ripple will be reflected in its input current (inductor current). Thus, an attentional should be paid to when designing the values of the inductor and the capacitors in accordance to maximum allowing low frequency ripple in the inductor current, to prevent the converter from operation in discontinuous conduction mode, where, the inductor current may reach zero ampere. Equation (3) shows the boundary that must be satisfied for any boost converter to operate in continuous conduction mode.

$$\frac{2Lf_s}{R_{critical}} > D(1-D)^2 \qquad (3)$$

Where, L is the inductance value of the inductor of boost converter and $R_{critical}$ is the equivalent output resistance that caused the boost to operate in discontinuous conduction mode.

III. Simulation Results

A simulation model is constructed to test and validate the performance of the proposed configuration. The output voltage of the multilevel inverter is shown Fig. 8. The voltage of each capacitor in the T-type multilevel inverter is controlled to be at 375V. Thus, the line-to-line output voltage is a five levels ($+2V_{dc}, +V_{dc}, 0, -V_{dc}$ and $-2V_{dc}$) stepped sinusoidal waveform with output levels (750V, 375V, 0V, −375 and −750V). Therefore, the peak output voltage is 750V multiplied by the modulation index mi = 0.8 at switching frequency f_s = 5kHz.

The capacitors voltages, three phase line-to-line output voltage and the three phase output currents in the motoring mode are shown in Fig. 10. Where the motor is represented by series RL load (R=5Ω and 1mH). The dc-dc stage is connected to the battery to boost its voltage from V_{dc} = 200V to 375V at duty cycle D = 0.53 at switching frequencyf_s = 50kHz.

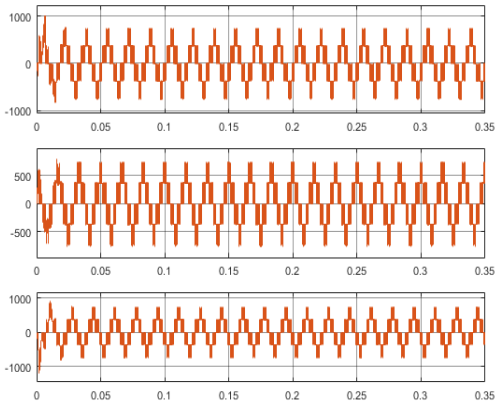

Fig. 8. Three phase line to line output voltage.

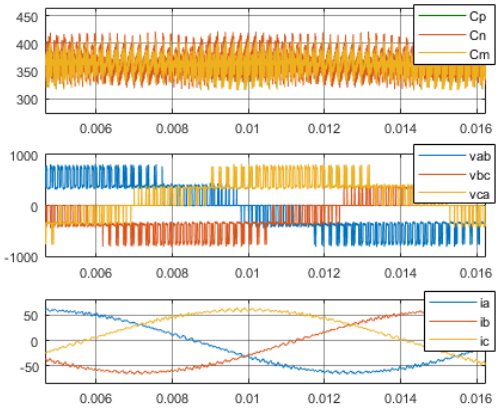

Fig. 9. Low frequency ripple on capacitors voltage Vcn, Vcm and Vcp in corresponding to the three phase output power; three phase output voltage; and three phase output current.

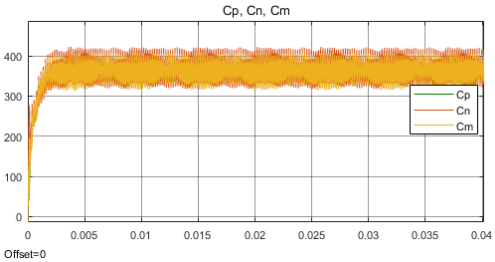

Fig. 10. Capacitor voltage at steady state.

The dc-dc stage inductor is 52 uH and the three capacitors and the input capacitor connected to the battery (used in bucking mode in regenerative mode) are equal and equal to 10uF / 400V which is in the range of film capacitors available

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in the market. A better sizing of the components of the proposed configuration (capacitors and inductors) can be achieved with optimized type three compensator that will provide an accurate control of the dc bus and hence reduces its voltage ripple.

Benefit from the capacitor voltage balance circuit the middle capacitor C_M charges the upper capacitor C_P as explained up to the output voltage of the boost converter $V_{CP} = V_{CM} = V_{CN}$. Fig. 10 shows the capacitors voltages at steady state operation where the converter is able to stabilize and equalize the output voltage of the capacitors $C_M, C_N,$ and C_P.

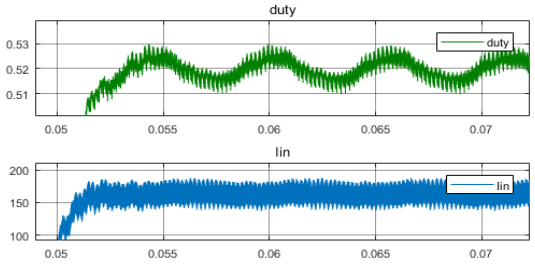
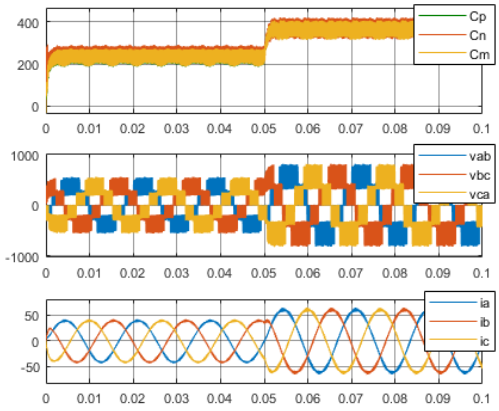


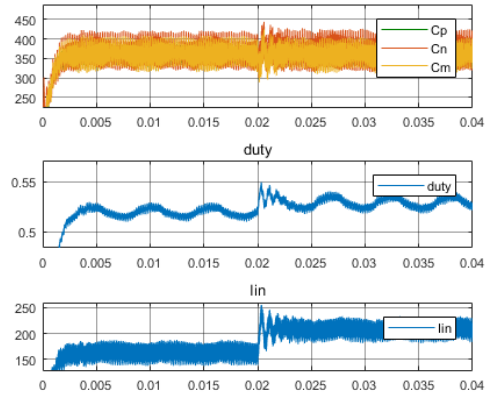
Fig. 11. Duty cycle of the dc-dc boost with the low frequency 180 Hz superimposed ripple; and inductor current at motoring mode.

Fig. 11 shows duty cycle of the dc-dc boost d and the inductor current i_L where the waveforms reflect the compensation of the dc bus variation due to the positive half cycle of the three-phase 180Hz ripple as shown in Fig. 6. Thus, low capacitance capacitors can be implemented and therefore replacing the short lifetime electrolytic capacitor with a long-life film capacitor. Moreover, it is important to note that either in boosting mode or bucking mode, all of the power switches experience a peak inverse voltage equal to half of the peak to peak output voltage ($V_{PIV} = V_{CP} = V_{CN} = 375V$). Therefore, compared to a conventional dc-dc converter, the proposed configuration implements power switches with a lower R_{ON} resistant which in return offers higher efficiency and better thermal properties.

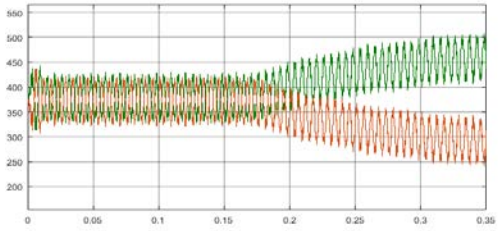
To validate the ability of the proposed configuration to balance the capacitors' voltages and to control the neutral point voltage at step change in the dc bus voltage or at fault condition. Fig. 12 (a) shows the converter response to a step change in the dc bus reference from 550V to 750V at $t = 0.05s$. The balance in be between C_n and C_p is reserved by C_m, keeping the symmetry of the ac output voltage levels and the balance of the ac output current. A fault has been introduced to the system by connecting a 20Ω resistor in parallel with the lower capacitorC_N. Fig. 12 (b) shows the capacitor voltage restoration after applying the fault condition at $t = 0.02s$. It can be notice that the ripple at the lower capacitor C_N has been transferred to the other two capacitors C_M and C_P. However, the dc-dc converter successfully restored the output voltage at its reference value while continues compensated for the excess power drain from the lower one, as can be seen in duty cycle and input current (inductor current i_L) in Fig. 12 (b). On contrary, with a conventional dc-dc converter when the same fault has been introduced, the capacitors' voltages continue to deviate from their reference values, as shown in Fig. 12 (c). This is due to that fact that, with a conventional dc-dc converter and T-type MLI, the capacitor ripples as 180° out of phase at all time, as shown in Fig. 7 (a). Thus, it can't be detected by the controller of the dc-dc converter. Hence, the voltage balance cannot be restored without extra control loops and sensors.



(a) Step change in the dc link voltage reference from 275V to 375V at t=0.05s; capacitors voltage Vcn, Vcm and Vcp; three phase output voltage; and; three phase output current.



(b) Capacitors voltage; dc-dc duty cycle; and the input current at fault condition by connecting 20 ohm resistor to Cn at t=0.02s.



(c) Voltage of C_P and C_N at fault condition in conventional configuration.

Fig. 12. The voltage of the converter's capacitor at step change and fault condition.

The performance of the proposed configuration is also tested in bucking mode to prove the bi-directional operation of the converter. Fig. 13 shows the three phase motor regenerative currents. While Fig. 14 shows the inductor current i_L at regenerative mode. The negative value indicate the reverse power flow from the motor (which acts now a generator) to the

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battery. The converter successfully is able to transfer the power in the reverse direction by bucking the DC bus voltage 750V to 375V and then to 190V. This is being done which keeping the capacitors' voltage balanced over the complete breaking cycle, as shown in Fig. 15.

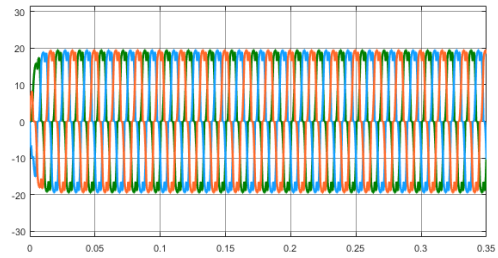


Fig. 13. Motor current in regenerative mode.

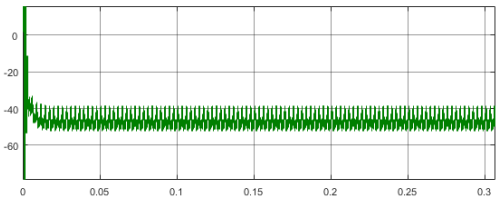


Fig. 14. Inductor current in regenerative

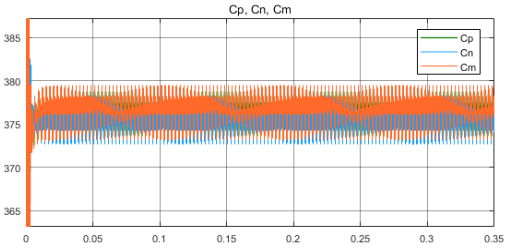


Fig. 15. Capacitor voltages in regenerative mode.

IV. Experimental Results

A laboratory prototype is built to test and validate the performance of the proposed configuration. Fig. 16 shows the experimental setup. Both bi-directional multilevel dc-dc converter and the T-type MLI uses A22N60AE power switches. The output capacitors of the bi-directional converter are 10 uF, 450V capacitors and its inductor is 1mH inductor wounded around N87E magnetic core.

Fig. 17 (a) shows capacitors' voltage V_{CN}, V_{CP} and V_{CM} in conjunction with the proposed converter line-to-line output voltage. The input voltage is boosted form 200V to 400V at $d = 0.5$ and switching frequency $f_s = 50\text{kHz}$. Fig. 17 (b) shows the capacitors' voltage ripple (oscilloscope channels in ac coupled mode) and the gating signal applied to Q1 and Q3 and its complementary applied to Q2 and Q4 as explained in section II. The capacitor's voltage V_{CN}, V_{CP} and V_{CM} are balanced cycle-by-cycle while their voltage ripple (due to high frequency switching $f_s = 50\text{kHz}$) is kept at 20V peak-to-peak at all time, despite the voltage ripple cause be converter's switching frequency 5kHz and triple line frequency ripple.

The three phase line-to-line output voltages (V_{ab}, V_{bc} and V_{ca}). of the proposed configuration output stage (T-type based MLI) is shown in Fig. 18 (a), which is constructed by connecting the load terminal to the upper capacitor C_P at the positive half cycle and to the lower one C_N at the negative half cycle. The zero voltage (freewheeling) state is achieved by clamping the load voltage by the bi-directional switch as mentioned earlier. Thus, a line-to-line 5 levels output voltage is achieved ($400V, 800V, 0V, -400V$ and $-800V$).

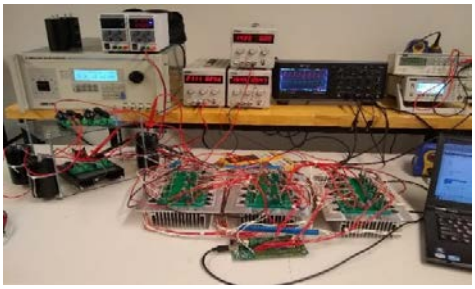
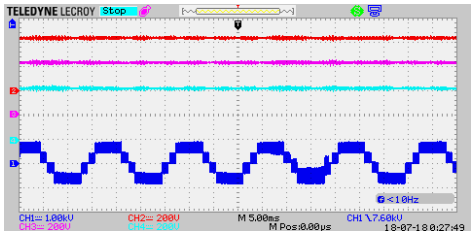
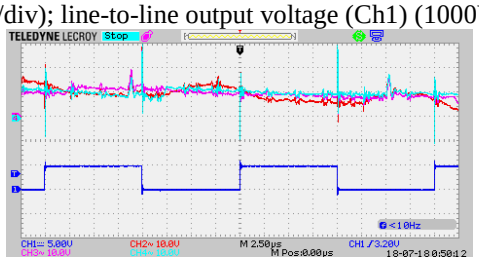


Fig. 16. Experimental setup



(a) Capacitor voltage V_{CN} (Ch2), V_{CP} (Ch3) and V_{CM} (Ch4) (200V/div); line-to-line output voltage (Ch1) (1000V/div).



(b) Capacitors voltages ripple (ac coupled) V_{CN} (Ch2), V_{CP} (Ch3) and V_{CM} (Ch4) (10V/div) against Q1 and Q3 gate signal (Ch1) (5V/div).

Fig. 17. Capacitor voltage of C_N, C_M and C_P

Fig. 18 (b) shows the three phase output current while suppling a $120\Omega, 80\text{mH}$ load. It is worth mentioning that, the peak inverse voltage of the power switches and capacitors are equal (400V) and limited to half of the dc bus voltage (800V) at the input of the multilevel inverter. It can be seen, that during the operation, the proposed configuration successfully maintained the capacitors' voltage and the dc bus voltage at their reference values. The experimental results are therefore matches the simulation results proving the validity of the proposed configuration in electric vehicles drive applications.

Furthermore, the proposed configuration is tested against fault conditions. A fault stimulation is introduced to the converter by connecting 20Ω resistor to the lower capacitor C_N and then disconnecting it periodically using a series external power switch.

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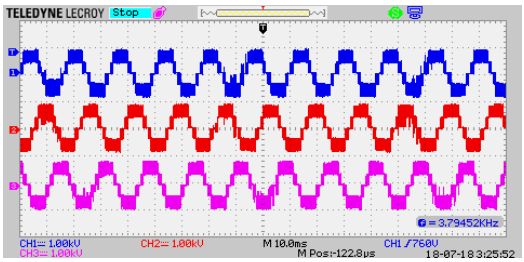
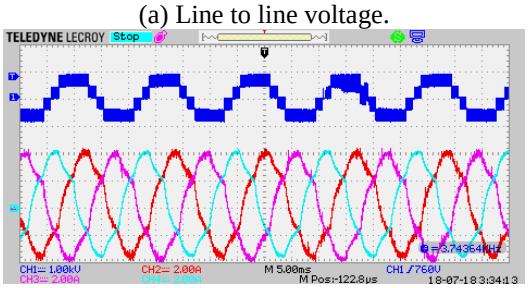
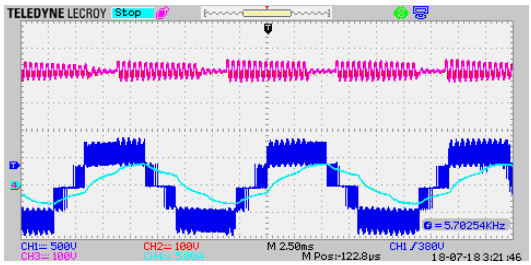


(a) Line to line voltage.

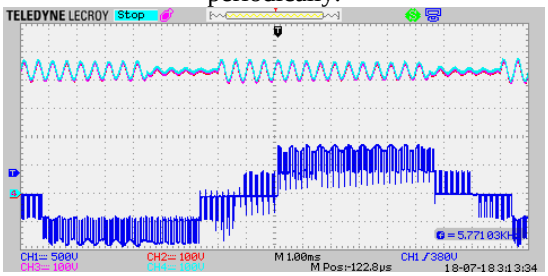


(b) Three phase output current.

Fig. 18. Multilevel output voltage of the T-type MLI.



(a) Capacitors voltage ripples V_{CN} (Ch2) and V_{CP} (Ch3) (100V/div) against line-to-line voltage (Ch1)(1000V/div) and phase current (5A/div) at applying a fault resistance (20Ω) periodically.



(b) Capacitors voltage ripples V_{CN} (Ch2), V_{CP} (Ch3) and V_{CM} (Ch4) (100V/div) against line-to-line voltage (Ch1)(1000V/div) at applying a fault resistance (20Ω) periodically.

Fig. 19. Capacitors' voltage ripple and ac output waveforms at fault conditions

Fig. 19 (a) shows the C_N and C_P voltage with respect to the converter output voltage and output current. Although the introduced fault caused an increase in their voltage ripple and due to the cycle-by-cycle balance this ripple is transferred to the upper capacitor as well C_P. The balance between the three capacitor is reserves during the test proving the ability of the proposed configuration as shown in Fig. 19 (b). Nonetheless, a better performance can be achieved with more optimized designed compensator (which controls the input boosting stage) which can better compensate and reduce the oscillation of the capacitors' voltages.

V. Conclusion

This paper presents a new integration of the five levels T-type multilevel inverter with a modified bi-directional dc-dc multilevel converter for electric vehicle applications. While the T-type MLI utilize more power switches compared to the conventional voltage source inverter. It generates a higher number of output voltage levels utilizing power switches with half of the peak inverse voltage. However, if such converter is connected to a conventional bi-directional dc-dc converter, the converter power switches have to be designed to withstand the full voltage of the dc bus. Moreover, such conventional configuration needs an addition of voltage balance circuit or special switching pattern with feedback and control loops to insure the voltage balance of the dc capacitors. On the contrary, the proposed configuration takes advantage of the high frequency cycle-by-cycle voltage balance between the dc bus capacitors C_N and C_P as explained in section II, these capacitors are designed according to the dc-dc input stage high frequency ripple not the line low frequency ripple at 180Hz (triple the rated frequency). Therefore, the required capacitance is reduced from several hundreds uF capacitors to tenth uF capacitors, allowing for replacing electrolytic capacitors with film capacitors. Such advantage of the proposed converter doesn't interfere with its ability to operate in step-up mode in motoring and in step-down mode in braking the electric motor. Moreover, the peak inverse voltage of all the power switches and the rated voltage of all capacitors is limited to half of the peak ac output voltage, which reduces the voltage stress and allow for implementing higher efficiency power switches in the dc-dc side similar to the ones in the T-type MLI side. The proposed configuration has been tested and validated though simulation model and experimental prototype. The results are compared and discussed, to demonstrate the advantages of the proposed configuration over the conventional one available in the market. In addition; efficiency levels are measured to be around 90%, which is far better than the market range. This work is to be extended by testing the proposed configuration against a complete EV driving cycle at low, medium and high speed to study evaluate the performance of operating EV with a higher rated voltage motors and its impact on the kWh per mileage consumption.

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